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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,800	04/09/2004	Meng-Jen Wang	WANG3237/EM	8707

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BACON & THOMAS, PLLC
625 SLATERS LANE
FOURTH FLOOR
ALEXANDRIA, VA 22314

EXAMINER	
TRAN, THANH Y	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,800	WANG, MENG-JEN	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-11 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barrett (U.S. 2003/0183934) in view of Reinikainen et al (U.S. 2003/0202332).

As to claims 1, 5 and 6, Barrett discloses in figure 3 a multi-chips stacked package, comprising: a substrate (330) having an upper surface, a lower surface and an opening passing through the upper surface and the lower surface; an upper chip (310) having a first active surface and a first back surface, wherein the upper chip (310) is flipped over and attached to the upper surface of the substrate (330) via a plurality of first electrically conductive bumps; a lower chip (350) accommodated in the opening and electrically connected to the first active surface of the upper chip (310) through a plurality of second electrically conductive bumps. Barrett does not teach the multi-chips stacked package comprising a reinforced bump interposed between the substrate and the upper chip; wherein the reinforced bump is located at a corner of the active surface of the upper chip; and wherein the reinforced bump is located at a periphery of the first active surface of the upper chip. Reinikainen et al discloses in figures 1-8, a multi-chips stacked package comprising a reinforced bump ("polymer ball" 120) interposed between the substrate (720) and the upper chip (700); wherein the reinforced bump ("polymer ball" 120) is located at a corner of the active surface of the upper chip (700); and wherein the reinforced bump ("polymer

ball" 120) is located at a periphery of the first active surface of the upper chip (700). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the package of Barrett by having a reinforced bump as taught by Reinikainen et al for improving mechanical compliance of the surface mount package to the substrate (see paragraph [0022] in Reinikainen et al); also supporting the upper chip mounted on the substrate.

As to claim 2, Barrett discloses in figure 3 a multi-chips stacked package, further comprising an under fill (320) filled into the opening.

As to claim 3, Barrett discloses in figure 3 a multi-chips stacked package, wherein the under fill (320) covers the first electrically conductive bumps and the second electrically conductive bumps.

As to claim 4, Barrett discloses in figure 3 a multi-chips stacked package, wherein the upper chip (310) covers the opening.

As to claim 7, Barrett discloses in figure 3 a multi-chips stacked package, wherein a solder bump is closed to the perimeter of the opening. Barrett does not disclose the package having a reinforced bump wherein the reinforced bump is closed to the perimeter of the opening. Reinikainen et al discloses in figures 1-8, a multi-chips stacked package comprising a reinforced bump ("polymer ball" 120) interposed between the substrate (720) and the upper chip (700). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the package of Barrett by replacing a solder bump which is closed to the perimeter of the opening with a reinforced bump of Reinikainen et al for improving

mechanical compliance of the surface mount package to the substrate (see paragraph [0022] in Reinikainen et al); also supporting the upper chip mounted on the substrate.

As to claims 8, 9, 11, Barrett does not the package having a reinforced bump, wherein the reinforced bump is a ring-like bump or a bar-like bump, or reinforced bump is a solder bump. Reinikainen et al discloses in figures 7 and 8 a package having a reinforced bump, wherein the reinforced bump is a ring-like bump or a bar-like bump, or reinforced bump is a solder bump. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the package of Barrett by replacing a solder bump with a reinforced bump having different shapes as taught by Reinikainen et al for improving mechanical compliance of the surface mount package to the substrate (see paragraph [0022] in Reinikainen et al); also supporting the upper chip mounted on the substrate.

As to claim 10, Barrett discloses in figure 3 a multi-chips stacked package, wherein the underfill (320) covers the solder bump. Barrett does not disclose the underfill covers the solder bump wherein the solder bump is a reinforced bump. Reinikainen et al discloses in figures 1-8, a multi-chips stacked package comprising a reinforced bump ("polymer ball" 120) interposed between the substrate (720) and the upper chip (700). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the package of Barrett by replacing a solder bump with a reinforced bump as taught by Reinikainen et al for improving mechanical compliance of the surface mount package to the substrate (see paragraph [0022] in Reinikainen et al); also supporting the upper chip mounted on the substrate.

As to claim 15, Barrett discloses in figure 3 a multi-chips stacked package, further comprising a plurality of solder balls (340) formed on the lower surface of the substrate (330).

As to claim 16, Barrett in view of Reinikainen et al do not disclose the reinforced bump is made of epoxy. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the package of Barrett in view of Reinikainen et al by using epoxy material for the reinforced bump for supporting the upper chip mounted on the substrate, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

As to claim 17, Barrett discloses in figure 3 a multi-chips stacked package, wherein the upper chip (310) is larger than the lower chip (350) in size.

As to claims 18, 19 and 20, Barrett discloses in figure 3 a multi-chips stacked package; wherein the underfill (320) covers a portion of the first active surface of the upper chip (310) or entirely covers the first active surface of the upper chip (310), or a portion of the upper surface of the substrate (330).

3. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormick (U.S. 6,558,978) in view of Reinikainen et al (U.S. 2003/0202332).

As to claims 21 and 23, McCormick discloses in figure 4 a multi-chips stacked package comprising: a substrate (402) having an upper surface and a lower surface; an upper chip (410) having a first active surface and a first back surface, wherein the upper chip (410) is flipped over and attached to the upper surface of the substrate (402) via a plurality of first electrically conductive bumps (as indicated at 414); a lower chip (412) interposed between the upper surface of the substrate (402) and the first active surface of the upper chip (410) and electrically connected to the first active surface of the upper chip (410) through a plurality of second

electrically conductive bumps (as indicated at 422). McCormick does not teach the multi-chips stacked package comprising a reinforced bump interposed between the upper surface of the substrate and the first active surface of the upper chip; and wherein each of the first electrically conductive bumps is substantially equal to the reinforced bump in height. Reinikainen et al discloses in figures 1-8, a multi-chips stacked package comprising a reinforced bump ("polymer ball" 120) interposed between the upper surface of the substrate (720) and the first active surface of the upper chip (700); and wherein each of the first electrically conductive bumps is substantially equal to the reinforced bump in height. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the package of McCormick by having a reinforced bump substantially equal to the first electrically conductive bumps in height as taught by Reinikainen et al for improving mechanical compliance of the surface mount package to the substrate (see paragraph [0022] in Reinikainen et al); also supporting the upper chip mounted on the substrate.

As to claim 22, McCormick discloses in figure 4 a multi-chips stacked package, wherein each of the first electrically conductive bumps (as indicated at 414) is larger than each of the second electrically conductive bumps (as indicated at 422) in height.

4. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barrett (U.S. 2003/0183934) in view of Reinikainen et al (U.S. 2003/0202332) as applied to claims 1 and 11 above, and further in view of Ho (U.S. 5,598,036).

As to claims 12 and 13, Barrett in view of Reinikainen et al do not teach the reinforced bump comprises lead and tin material; and wherein the ratio of the lead and the tin is 95:5. Ho (U.S. 5,598,036) teaches the package in figures 2-6 comprising a reinforced bump (26) for

supporting the upper substrate mounted on the PCB (20); wherein teach the reinforced bump (solder joint 26) comprises lead and tin material (see col. 4, lines 8-23 and lines 54-60); and wherein the ratio of the lead and the tin is 95:5 (see col. 4, line 54 - col. 5, line 8). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the package of Barrett in view of Reinikainen et al by using lead and tin material for a reinforced bump as taught by Ho. One of ordinary skill in the art would have been motivated because using lead and tin material for a reinforced bump would provide a high melting solder (see col. 4, lines 39- col. 5, line 8 in Ho).

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barrett (U.S. 2003/0183934) in view of Reinikainen et al (U.S. 2003/0202332) as applied to claims 1 and 2 above, and further in view of Degani et al (U.S. 5,608,262).

As to claim 14, Barrett in view of Reinikainen et al do not disclose the lower chip has a second back surface exposing out of the underfill. Degani et al discloses in figure 10 a package comprising a lower chip (17) having a second back surface exposing out of the underfill (22). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the package of Barrett in view of Reinikainen et al by having a lower chip having a second back surface exposing out of the underfill as taught by Degani et al for reducing the package's weight and production cost.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wenzel et al (U.S. 6,150,724), Dore et al (U.S. 6,239,484), Bozso et al (U.S. 5,760,478), Harper et al (U.S. 6,659,512), Degani et al (U.S. 6,369,444), Gupta et al (U.S. 5,198,963), and Kelkar et al (U.S. 6,084,308) disclose prior arts relevant to the invention.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800